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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
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Dsp-based bit clock recovery

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DSP-based bit clock recovery

Field of the Invention

The invention relates to the data acquisition in digital storage media readout.

Background

Information readout from digital storage media with moving parts always involves the task of recovering the bit clock from the incoming time-continuous readout signal. Only with a reliably known bit clock can the readout signal be converted into a sequence of bits, and thus be ready for subsequent time-discrete, fully digital processing.

Additionally, whenever a specific storage media format foresees to group information into a repetitive pattern of data frames of predefined layout, also denoted as sync frames, the alignment of the data relative to this pattern has to be recovered. This is also denoted as sync frame alignment recovery. A related task, especially important during random access, is to verify from the read data which of the frames currently is being read, which is also denoted as readout address recovery. Sync frame alignment recovery and readout address recovery are made possible by concepts where e.g. every sync frame begins with a dedicated sync pattern and this sync pattern is additionally suffixed with an address information. The sync pattern together with the subsequent address information often is denoted as sync code.

Additionally, whenever a storage media readout device is compliant to more than one storage media types or formats, the device has to recognize the media type at an early stage after media insertion, in order to be able to perform

any subsequent data handling in accordance with the specification(s) relevant for that specific type of media.

An apparatus according to the present invention performs one or more of the following functions:

- To recover the bit clock during digital storage readout,
- To recover the sync frame alignment of the data,
- To decode, as early as possible, addressing information contained in the data,
- To recognize the type of media that is being accessed.

The concepts of the invention are advantageously applicable in other fields of digital technology like receiving digitally transmitted signals.

An approach for bit clock recovery is a Phase-Locked Loop (PLL); in case of optical media like Compact Disk (CD), Digital Versatile Disk (DVD) or Blu-ray Disk (BD), a digital PLL can be employed.

Invention

According to this invention, bit clock recovery is performed using the following steps in sequence:

a.) A sequence of A-to-D-converted samples representing an oversampled readout signal from the storage medium is stored in a memory.

b.) The stored sample sequence is scanned for occurrences of one or more predefined sync patterns. The positions of found occurrences are memorised as sync positions. For this scanning, e.g. a cross-correlation algorithm can be employed.

c.) The distance between consecutive sync positions is measured.

d.) From the distance of sync positions and the known sync frame structure, the base frequency of the samples is calculated. From the sync positions and the base frequency, the bit clock is regenerated.

e.) Using the regenerated bit clock, the sample sequence from memory is sample rate converted into a new sequence, which represents the readout signal when sampled at the correct bit clock rate.

This has the general advantage that the power and area consuming implementation of a sophisticated and complex digital PLL is conceptually avoided.

Advantageously, bit clock recovery according to this invention may additionally comprise the following step:

- Whenever an occurrence of a sync pattern has been found, the associated sync code is decoded by a pattern recognition algorithm.

This has the advantage that sync codes can be detected and the position of the read unit be determined at a very early stage in signal processing. Any PLL locking is not required. Hence the sync code decoding step proposed in the invention is very fast, which is advantageous during random access mode.

Advantageously, bit clock recovery according to this invention may additionally comprise the following step:

- From the distance between consecutive sync positions and the knowledge about which type of sync pattern has been found, recognize the format of the storage media (e.g. CD, DVD, BD).

This has the advantage to constitute a very reliable media recognition, because it is exclusively based on details of the physical recording format that are fixed. It does not rely upon storage media material properties, which may vary. In case of optical disks, the reflectivity is known

to vary across media brands and even across manufacturing lots; hence a media recognition based on reflectivity measurement is error prone. Another advantage is that, being located in very early stages of signal processing, media recognition is considerably faster than any methods based on evaluating disk reflectivity and/or focus position.

The present invention provides the following advantages:

- The proposed algorithms to recover the bit clock from a set of samples can easily be adapted, even during operation, to the type of optical media, the applied channel modulation method and the actual drive speed. Therefore, it is possible to use different algorithms for each type of media in order to reduce the bit-error-rate of the read channel.
- It is even possible to first detect, using concepts of this invention, the type of media, and then to switch to one of a set of optimised algorithms of this invention for bit clock recovery and/or sync alignment.
- In this way, the invention offers improved flexibility in handling different media.

With other words, the invention describes a bit clock recovery apparatus for digital storage readout employing sync frames, where an oversampled readout signal is stored in memory, sync patterns are located in the signal using DSP means, distances of consecutive sync pattern locations are calculated, and bit clock is recovered from these distances and the knowledge about the data framing structure.

Brief description of the drawings

Fig. 1 shows in block diagram form the classical approach for clock recovery.

Fig. 2 shows in block diagram form an implementation of clock recovery and sample rate conversion according to the invention.

Fig. 3 shows the parallelisation approach for sample rate conversion.

Fig. 4 shows in block diagram form the required enhancements to implement Sync ID decoding according to the invention.

Exemplary embodiments

Bit clock recovery is one of the main problems for the implementation of an acquisition path of digital storage readout devices. Main target of the clock recovery is the determination of the actual channel bit rate from a sampled time-continuous read signal. This clock recovery has to deal with a wide range of channel bit rates because of different media (CD, DVD, DVR) and different read speeds. Today, the channel bit rate varies from 4.12 Mbit/s (CD 1x) to 400 Mbit/s (DVD 16x). In the near future, 500 Mbit/s for DVD 20x have to be expected.

Most optical discs are recorded or pre-recorded with a constant linear velocity (CLV) mode. This implies that for a nominally constant channel bit rate, a higher rotational speed is required when reading near the inner radius of the data area, and a lower rotational speed at the outer radius, and that rotational speed must be adapted whenever the readout radius changes. Because rotation speed adaptation is never perfect or instantaneous, momentary

channel bit rate will vary during read of the entire disc and after jumps from one sector to another.

Fig. 1 shows the classical approach for clock recovery. This approach is based on an ADC, a digital PLL, a Sample Rate Converter (SRC), and the channel bit decoding unit. The digital PLL is used to derive the actual channel bit rate and a phase information from the samples of the analogue signal. Because this PLL has to lock to a wide range of bit clock rates and various different bit patterns with various different modulations for CD, DVD and, in future, DVR, the implementation of this PLL is a very sophisticated and complex task. Main input signal for the digital PLL is a phase information from the channel bit decoding unit. The digital PLL is locked if this signal becomes zero.

The SRC uses the signals from the digital PLL, namely frequency and phase information, to convert the physical samples into virtual ones, which correspond to the actual channel bit rate.

Fig. 2 shows an implementation of clock recovery and sample rate conversion according to the invention. First, a number of n consecutive samples from the ADC are stored in a FIFO. Same as with the classical approach described above, the sample rate of the ADC has to be at least equal to the maximum channel bit rate, as taught by Shannon's sampling theorem. The size of the FIFO should be large enough to store all samples between and including two consecutive sync patterns.

In parallel, the actual channel bit rate for this set of samples is determined by the measurement of the distance between two consecutive sync patterns. In one form or

other, such sync patterns exists for all optical storage media (CD, DVD, DVR).
Because the expected sample sequence for the sync pattern is known in advance, the required sync pattern detection can be based on algorithms like cross-correlation. From the distance between two consecutive sync patterns, the actual channel bit rate of the samples stored in the FIFO is calculated.

In a third step, the samples are converted to the calculated channel bit rate by the sample rate conversion unit, i.e. based on an interpolation algorithm.
As an advantage, this kind of sample rate conversion can be implemented in an integrated circuit with highly parallel hardware structures, such that high clock rates are avoided. Fig. 3 shows this parallelisation approach. The samples from the ADC are clocked into n FIFOs connected to n SRC units. Because every SRC unit now has to handle only every n-th set of samples, the throughput constraints are relaxed significantly. This results in a lower clock speed for the SRC units.
Because the input FIFO processing speed is independent of the sample rate of the ADC, the SRC units can be clocked independently from the ADC. This is an advantage for high speed drives, were clock rates up to 300 MHz for the ADC are required. If channel bit rate calculation and sample rate conversion are designed to handle 4 samples per clock, the required clock speed for these units would be 75 MHz only.

After the determination of the length of the sync codes (measured in number of HF samples) and the distance of two consecutive sync codes (also measured in number of HF samples), the length of a channel bit in the HF signal is also known in terms of HF samples.

For the channel bit clock recovery, it is sufficient to detect the unique portion of the sync code. This is a 9T/9T signal for the BD format, a 14T signal for DVD and an 11T/11T signal for CD. Based on the information from the sync code detection, mainly the position of the sync code, a simple decoding of the non-unique portion of the sync codes can also be implemented. This decoding can be done based either on the HF signal or advantageously, as shown in Fig. 4, on the resampled signal. Because only a limited set of valid sync code exists for each format, a maximum likelihood decoder may be applied.

In a favourable extension, media recognition can also be achieved based on cross correlation: First, the cross correlator is programmed for the detection of a specific type of sync codes. This is a 9T/9T signal for the BD format, a 14T signal for DVD and an 11T/11T signal for CD. The possible range of the length of the sync codes is known from the current speed of the drive and the assumed format. A search for sync codes is then performed, e.g. an exhaustive search starting with the maximum possible sync code length and stepwise refining the cross correlator programming down to the minimal possible length. Media recognition is considered successful as soon as periodic sync codes are detected, i.e. as soon as a fixed distance is found between any two consecutive sync codes. If no periodic sync codes can be detected throughout the complete search, the media does not comply to the media type of the sync code under investigation, the cross correlator has to be reprogrammed for the detection of another type of sync codes and the above described procedure has to be repeated.

Claims

1. An apparatus for recovering the channel bit clock in the readout part of a digital storage system compliant to a range of one or more digital storage formats each having a specific channel bit clock and framing structure, comprising sampling and analogue to digital conversion means, sync pattern detection means and sample rate conversion means, **characterised** in that
   - the digital storage readout signal is sampled at a frequency at least as high as the maximum of all channel bit clocks among the range of formats,
   - the sampled readout signal is analysed to locate occurrences of one or more predefined sync patterns,
   - the channel bit rate and/or the channel bit clock are calculated from the locations where sync patterns have been located, and
   - the sampled readout signal is converted to the sampling rate defined by the calculated channel bit clock.

Abstract

DSP-based bit clock recovery

A bit clock recovery apparatus for digital storage readout employing sync frames, where an oversampled readout signal is stored in memory, sync patterns are located in the signal using DSP means, distances of consecutive sync pattern locations are calculated, and bit clock is recovered from these distances and the knowledge about the data framing structure.

(Fig. 2)

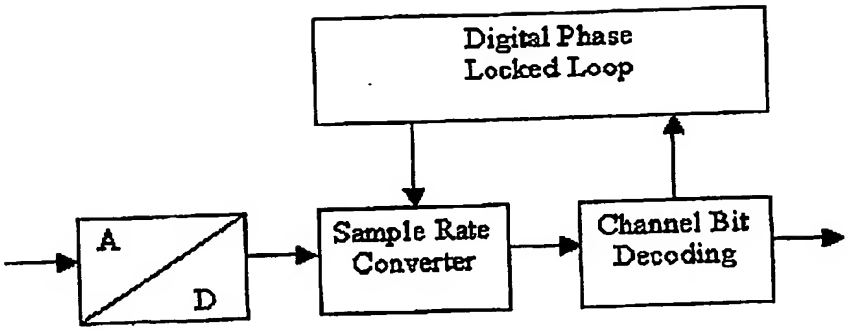

Figure 1

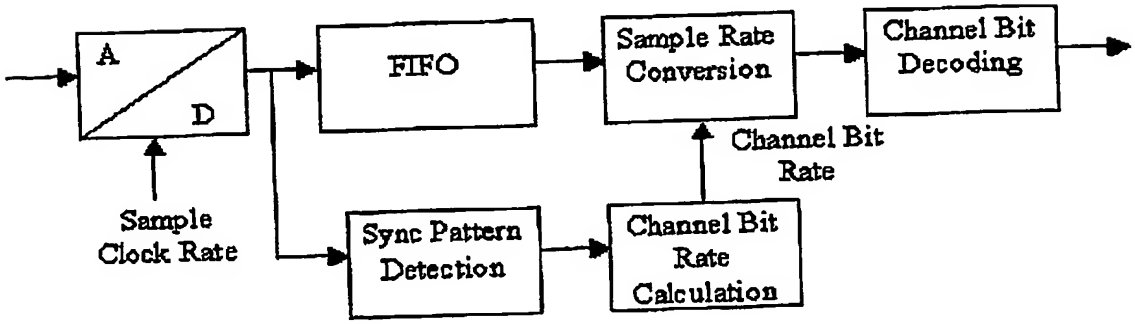

Figure 2

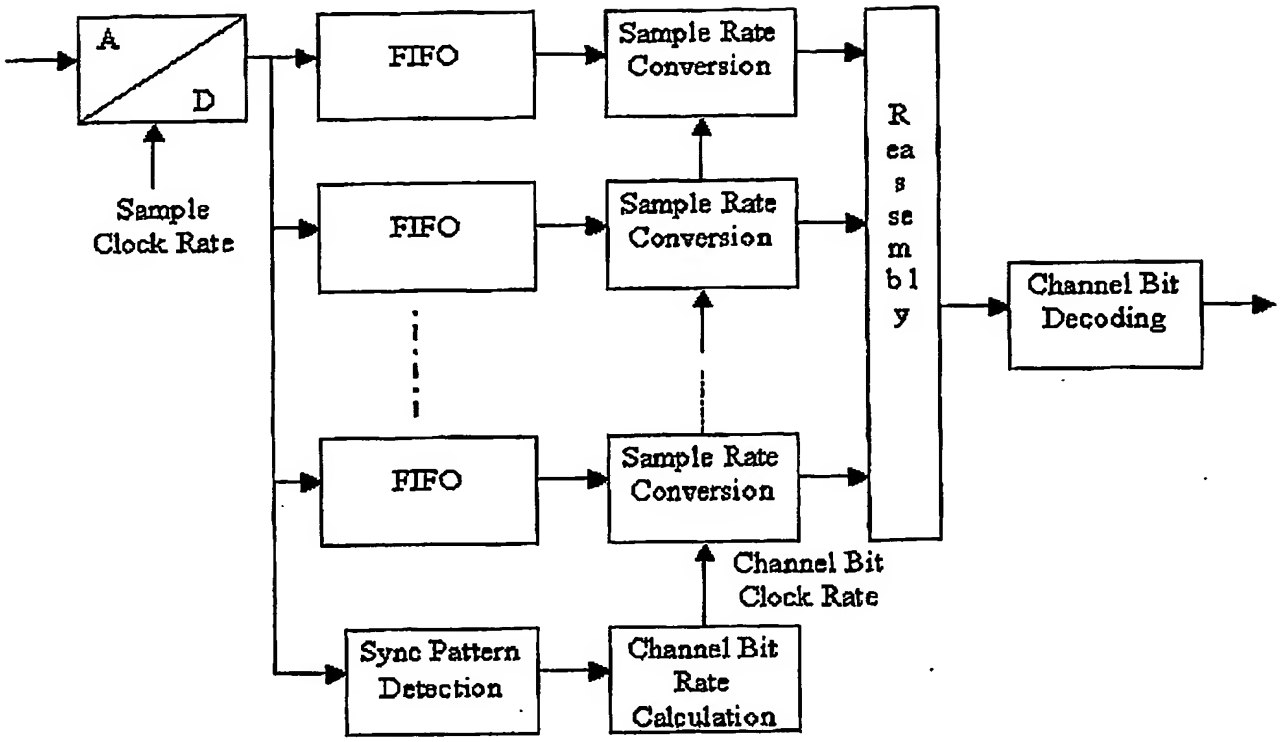
A
D
Sample Clock Rate
FIFO
FIFO
FIFO
Sample Rate Conversion
Sample Rate Conversion
Sample Rate Conversion
Reassembly
Channel Bit Decoding
Channel Bit Clock Rate
Sync Pattern Detection
Channel Bit Rate Calculation

Figure 3

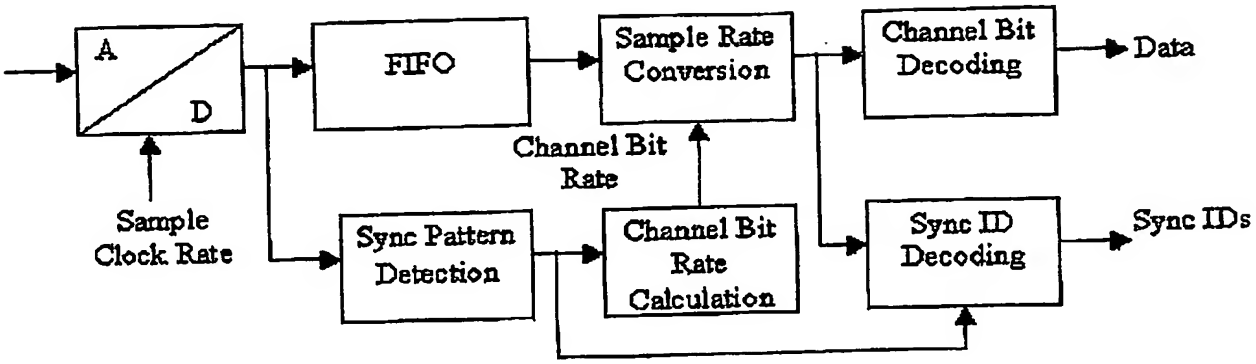
A
D
FIFO
Sample Rate Conversion
Channel Bit Decoding
Data
Channel Bit Rate
Sample Clock Rate
Sync Pattern Detection
Channel Bit Rate Calculation
Sync ID Decoding
Sync IDs

Figure 4